AF / GP2836
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PATENT

43269

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	
Stephen Liscinsky	:	Appeal No. _____
Serial No.: 10/085,138	:	Patent Art Unit: 2836
Filed: March 1, 2002	:	Examiner: Kito, Zeev
For: A THREE PHASE SUPERVISORY CIRCUIT	:	

REPLY TO EXAMINER'S ANSWER

Peter L. Kendall
Reg. No. 46,246
Roylance, Abrams, Berdo & Goodman, L.L.P.
1300 19th Street, N.W., Suite 600
Washington, D.C. 20036
(202) 659-9076

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REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

For the appeal to the Board of Patent Appeals and Interferences from the decision of August 5, 2003 finally rejecting claims 1-18 in the above-identified application, Appellant submits the following reply brief in response to the Examiner's Answer of May 5, 2004 in accordance with 37 C.F.R. § 1.193(b)(1).

I. Real Party in Interest

There is no dispute as to the real party in interest.

II. Related Appeals and Interferences

There is no dispute as to related appeals and interferences.

III. Status of the Claims

There is no dispute as to the status of the claims.

IV. Status of the Amendments

There is no dispute as to the status of the amendments after final.

V. Summary of the Invention

There is no dispute as to the summary of the invention filed with appellant's brief on appeal.

VI. Issue for Review

There is no dispute as to the issue for review in the appeal.

VII. Grouping of the Claims

There is no dispute as to the grouping of the claims filed with appellant's brief on appeal.

VIII. Claims Appealed

There is no dispute as to the status of the claims appealed.

IX. Prior Art of Record

There is no dispute as to the prior art of record.

X. Grounds of Rejection

In the Examiner's Answer, the Examiner maintains the rejection of claims 1, 4 - 6, 11, 12, 14 - 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 3,535,591 to Holmquest in view of U.S. Patent 5,224,010 to Tran et al. Claims 8 - 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of U.S. Patent 5,642,052 to Earle. Claims 2 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Aller, 105 USPQ 233. Claims 3 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Bosch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

XI. Argument

The Examiner's Answer appears to be based on a misunderstanding of the Holmquest patent and the Tran patent. The Appellant will elaborate on the operation of the circuits disclosed in the Tran patent and the Holmquest patent. Specifically, operational differences will be discussed in order to clarify any misunderstanding.

The Examiner contends that, in the Holmquest patent, the output of the sensing circuits are being delayed by a delay circuit based on elements 12-14 in FIG. 1 and element 22 in FIGS. 1 and 2. However, it is the Appellant's understanding that the system disclosed in the Holmquest patent does not delay the output of the sensing circuits, as does the Appellant's claimed invention. Rather the Holmquest patent, in column 4, lines 32 to 33 thereof, discloses a time delay in operation of relay 23 which is preset but variable as a function of input parameters. That is, the sensing circuits as disclosed in the Holmquest patent monitor the AC input signal for faults. If the faults continue for a predetermined

period, then relay 23 is deenergized. Relay 23 can only be energized if errors no longer exist on the AC input line.

The Examiner cannot only rely on the figures of the Holmquest patent, but must consider the supporting specification. In this case, the text goes against what the Examiner contends.

The Holmquest patent further discloses in column 1 lines 55 to 59 thereof:

> Voltage from the three phase power source to be monitored is fed into the system and any error detected by any one or more of the sensing circuits produces an error signal which is fed into a common logic and time-delay circuit. The logic and timing circuit controls the operation of a normally closed relay switch interposed in an output circuit of the monitoring system.

Thus, the sensing circuits are not being delayed. Instead the closing of the relay is being delayed. For example, if a fault is detected for a second, the relay may not be denergized. However, if the fault occurs for three seconds, the relay may be deenergized.

It is also the Examiner's contention that the Tran patent discloses delaying the outputs of the sensing circuits in the same manner as Appellant's claimed invention. However, this contention is incorrect. As claimed in claim 1 of Appellant's application, an activation circuit requires indication signals from both sensing and delay circuits comprising a delay signal and a sensing signal.

The power supply supervisory circuit disclosed in FIG. 2 of the Tran patent shows two delay circuits – a powergood driver 34 and a shutdown driver 38. Both delay circuits receive signals from the sensing circuits. Either one of the delay circuits issues a signal after delaying the received signals.

In contrast, Appellant's claimed invention provides a sensing signal and a delay signal via delay circuit 106 to the activation circuit 108. It should be appreciated, that after a predetermined time has elapsed, the delay circuit 106 provides a delay signal. It is the receipt of the sensing signal and the delay signal that provides an indication for the activation circuit to activate. Thus, the activation circuit requires both types of signals in order to operate. All of the Appellant's independent claims recite this aspect of the invention.

The Examiner also contends that the combination of the Tran patent and the Holmquest patent makes Appellant's invention obvious. As previously discussed, the Holmquest patent does not disclose delaying an output of the sensing circuits. The Examiner alleges that the circuit disclosed in the Tran patent can be used with the alleged teaching of the Holmquest patent to provide a delay for the sensing circuits. However, the delay disclosed in the Holmquest patent applies to the delay in the operation of a relay and not to a delay in the output of the sensing circuits. The Examiner is inappropriately taking portions of the two references to accomplish Appellant's invention using hindsight.

A prima facie obviousness determination requires a showing of the motivation to combine the teachings of the prior art to obtain the claimed method or apparatus. *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999). Obviousness cannot be established by showing that the teachings can be combined, where the motivation to make the combination is lacking. Obviousness requires a showing that one skilled in the art would be lead to make the proposed modification in the manner proposed by the Examiner.

The Examiner should be aware that the system disclosed in the Holmquest patent and the invention disclosed in Appellant's application are both used in high voltage settings. However, the circuit disclosed in the Tran patent is used in a low voltage environment. Specifically, the circuit disclosed in the Tran patent is described as being used to protect

integrated circuits such as, for example, CMOS circuits. More specifically, the circuit disclosed in the Tran patent is described as being used for a CPU. Hence, the requirement for monitoring DC voltages from a DC voltage supply. As is commonly known, ICs are sensitive to voltage fluctuations. Therefore, there is a need to monitor the DC input values to the ICs. The application of this low voltage circuit to the Holmquest high voltage system *is not* obvious.

With respect to the Tran patent, the delay circuit delays the application of DC power from an external power supply to microprocessor-type circuitry during the powering up period of the external supply when the supply's output is ramping up or switching from 0 volts to its specified level. After the power-up period, the Tran patent circuit delays the shutting down of the external power supply because of any subsequent fault the external supply may exhibit during the time it is supplying power to the connected circuitry. The claims invention does not employ a for the purposes of allowing the external AC power to ramp up and stabilize. It is contemplated that the external AC power will be at its nominal level. If it is not, the invention will not allow power to be switched to the loads regardless of a delay time. The delay is intended to allow the capacitors and related components in the invention's internal power supply and sensing circuits to ramp up and stabilize. By this action, the invention will switch power to the load accurately. The delay circuit of the invention will not come in to effect upon the presence of any fault on the AC power inputs, whether they are over or under voltages, open supply lines, etc. The circuit will shut down power immediately.

The Examiner also contends that the Holmquest patent and the Earle patent disclose a polyphase testing system. The Examiner is correct in that the title of the Holmquest patent refers to a polyphase system. However, the polyphase term used in the Holmquest patent title refers to an AC input signal. The Holmquest patent discloses under- voltage sensors for each

of the three phases. However, there is only one phase sensor. Therefore, the system disclosed in the Holmquest patent can only detect a problem with one of the three phases and cannot distinguish problems **between** the phases.

Similarly the Earle patent discloses a single phase testing system and not a multiphase testing system. For example, the testing system disclosed in the Earle patent cannot test whether "the ground and neutral lines are reversed, or if two hot wires have been connected to the receptacle or if a ground path exists, but is of poor quality, the tester may not detect such conditions" (see Col. 4, lines 54-58).

XII. Conclusion

For the reasons discussed above, the combination of the cited art does not disclose or suggest the claimed invention, that is the use of both sensing and delay circuit indication signals for an actuator circuit in a three phase supervisory circuit, among other features. The primary cited reference, Holmquest does not teach delaying an output of a sensing circuit. Rather, the Holmquest patent teaches delaying the deenergization of a relay. The Tran patent teaches the delay of an output of a sensing circuit receiving a DC input but not the use of signals from both sensing and delay circuits as indicator signals as claimed. Furthermore, the circuit disclosed in the Tran patent is applicable to a low voltage environment (e.g., ICs), and not to a high voltage environment. Accordingly, the rejection of claims 1-18 is untenable. Reversal of the final rejection is requested.

Respectfully submitted,

Peter L. Kendall
Reg. No. 46,246

Roylance, Abrams, Berdo & Goodman, L.L.P.
1300 19th Street, N.W., Suite 600
Washington, D.C. 20036
(202) 659-9076

Dated: July 6, 2004

APPENDIX A- COPY OF CLAIMS ON APPEAL

1. A three phase supervisory circuit for detecting fault conditions in an input AC power signal, comprising:

a first sensing circuit for detecting a voltage level for a first phase of said AC power signal and comparing said voltage level of said first phase to a threshold value;

a second sensing circuit for detecting a voltage level for a second phase of said AC power signal and comparing said voltage level of said second phase to said threshold value;

a third sensing circuit for detecting a voltage level for a third phase of said AC power signal and comparing said voltage level of said third phase to said threshold value;

a delay circuit for delaying initial operation of said sensing circuits for a predetermined period each time said supervisory circuit is powered on; and

an activation circuit for receiving indication signals from said sensing and delay circuits, said indication signals indicative of whether said predetermined period of time has elapsed and said voltage levels of said phases have met said threshold value.

2. The three phase supervisory circuit of claim 1, wherein said predetermined time period is approximately between one and two seconds in duration.

3. The three phase supervisory circuit of claim 1, wherein said threshold value is about 12 volts.

4. The three phase supervisory circuit of claim 1, wherein said indication signals represents at least one condition selected from the group consisting of:

a first positive indication that said input AC signal meets the threshold value;

a second positive indication that said predetermined time period elapsed;

a first negative indication that said input AC signal does not meet the threshold value; and

a second negative indication that said predetermined period of time does not elapse.

5. The three phase supervisory circuit of claim 1, wherein said predetermined period of time provides for stabilization of capacitors in said three phase circuit upon initially powering said three phase supervisory circuit.

6. The three phase supervisory circuit of claim 4, wherein in response to receiving said first and second positive indication signals said activation circuit outputs an AC power signal.

7. The three phase supervisory circuit of claim 6, wherein each of said sensing circuits has to detect a proper voltage level in a respective phase before a positive indication is provided to said activation circuit.

8. The three phase supervisory circuit of claim 1, further comprising a contactor coil connected to said activation circuit and a plurality of ground fault circuit interrupter (GFCI) receptacles.

9. The three phase supervisory circuit of claim 8, wherein said GFCI receptacles are protected from AC faults via said three phase supervisory circuit.

10. The three phase supervisory circuit of claim 1, wherein said three phase supervisory circuit operates as a tester for allowing testing of AC power signals.

11. The three phase supervisory circuit of claim 1, wherein said fault conditions comprise at least one of a phase reversal, a phase loss and undesirable changes in a phase voltage level.

12. A method for detecting fault conditions in an input AC power signal via a three phase supervisory circuit, the method comprising:

detecting a voltage level for three phases of said AC input power signal;

comparing said detected phase voltage levels to a threshold value;

delaying initial operation of sensing circuits of said three phase supervisory circuit for a predetermined period each time said supervisory circuit is powered on; and

providing results from said steps of comparing and delaying to an activation circuit.

13. The method of claim 12, wherein said predetermined period is approximately between one and two seconds in duration.

14. The method of claim 13, wherein said predetermined period occurs each time said three phase supervisory circuit is initially powered.

15. The method of claim 12, wherein said threshold value is about 12 volts.

16. The method of claim 12, further comprising:

providing an output AC signal upon a determination that no fault conditions were found in said AC input signal.

17. A three phase supervisory circuit for detecting fault conditions in an input AC power signal, comprising:

a first sensing circuit for detecting a voltage level for a first phase of said AC power signal and comparing said voltage level of said first phase to a threshold value;

a second sensing circuit for detecting a voltage level for a second phase of said AC power signal and comparing said voltage level of said second phase to said threshold value;

a third sensing circuit for detecting a voltage level for a third phase of said AC power signal and comparing said voltage level of said third phase to said threshold value;

a delay circuit for delaying operation of said sensing circuits for a predetermined period of time;

an activation circuit for receiving indication signals from said sensing and delay circuits, said indication signals indicative of whether said predetermined period of time has elapsed and said voltage levels of said phases have met said threshold value; and

at least two of said sensing circuits being operable to detect said fault conditions said fault conditions being selected from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of said phases.

18. A method for detecting ground fault conditions in an input AC power signal via a three phase supervisory circuit, the method comprising:

detecting a voltage level for three phases of said AC input power signal;

comparing said detected phase voltage levels to a threshold value;

delaying operation of said three phase supervisory circuit for a predetermined period;

providing results from said steps of comparing and delaying to an activation circuit; and

determining the existence of said fault conditions from said steps of comparing said detected phase voltage levels, said fault conditions being selected from the group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of said phases.